Design of Hybrid full adder Topology using Modified Triplet Logic

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ABSTRACT

In the recent era, area and power reduction procedure is gaining most attention for achieving minimum energy consumption. Full adder is the primary computational arithmetic block in numerous of the computing executions and hence is the critical component of ALU. Various existing full adders proposed in literature fail to accomplish low power delay product (PDP) and lacks driving strength when used in chains structure. In this project a novel 14T hybrid full adders have been proposed to reduce to area and power consumption. In addition the proposed full adder deign is implemented in 4 bit ripple carry adder chain structure to improve the driving strength and reduce the overall silicon area utilization and net power consumption. All the simulations will be carried out using Tanner with 45nm technology.

I. INTRODUCTION

Arithmetic operations, ALU is used as processing element inside the device. Full adder is the primary architecture of ALU and hence improving the performance of full adder is an important point of concern. High speed and low power full adder are essential in achieving high performance battery operated electronic devices. Many logic styles are used in designing full adders using GDI techniques previously. In the dynamic logic style clock signals are given to the NMOS and PMOS transistor. XOR-XNOR techniques have been realize high-speed and high-performance hybrid XOR-XNOR full adders. The full adder circuits based on 4T XOR-XNOR functions have a simple structure and reduced power consumption. The 14T FA designs have overcome non swing problem prevailing in the reported designs at low voltage and subsequently improved the performance of the circuit. This design reduces propagation delay and area of digital circuits while maintaining low complexity.

II. LITRETURE REVIEW

1.Area and Power Efficient Carry Select Adder using 8T Full Adder B. Sathyabhama, M. Deepika, and S. Deepthi, 2019

In this paper 8T full adder is used as a building block for 8-bit SQRT CSLA. 8T full adder is designed by XNOR hybrid CMOS design. To perform fast arithmetic operations, carry select adder is one of the fastest adders which is used for the processing of data complex.. The SQRT CSLA consists of 8T XNOR full adder. By using the Pass Transistor Logic, 8T XNOR full adder is performed. SQRT CSLA is constructed by equalizing the delay through two carry chains. To achieve low power consumption 8T FA is used as the building block for ripple carry adder. A hybrid CMOS full adder with 8T is constructed by using 3T XNOR circuit. Since XNOR consists of 3 transistors only. Figure.2.1, shows the 3T XNOR circuit. This 3T XNOR is designed using pass transistor logic (PTL). It is a highly compact design. XNOR operation is performed twice in 8T full adder and by using multiplexer, sum and carry were determined. The key factor for high speed design is the number of P-transistors should be less than N-transistor.

2. A Competent Design of 2:1 Multiplexer and Its Application in 1-Bit Full Adder Cell Amit Dubey Sachin Dubey Shyam Akashe, 2020

An architecture of 2:1 Multiplexer has been proposed. As we know that Multiplier is also known as MUX. In terms of consumption of power, temperature, delay and load capacitance of output, MDCVSL gives the good result by the addition of double weak P channel. In terms of delay, consumption of power and load capacitance of output the modified multiplexer of DCVSL 2:1 gives the better result. In the MDCVSL, the

connection of six NMOS and the four PMOS is done and single addition of supply is utilized on the circuit for switching. VPULSE is connected on every input port out of six input on which we find out the fall time, rise time, voltages V1 and V2, time period and width of pulse and Z and Zb is connected at the two output port and at the ground port GND is connected in the circuit.

3. 1-Bit Hybrid Full Adder by GDI and PTL Technique Kshitij Shant, Rita Mahajan, 2019

In this paper 1 bit full adder hybrid circuit has been proposed which consist of two techniques i.e. Pass transistor Logic and Gate Diffusion Technique. A single bit full adder cell is designed to represent the efficiency of the proposed architecture. For the designing of low power the method (GDI and PTL) is used. The typical complication in PTL and GDI technique is that the swing output is less because the Vdc is not included in the Gate Diffusion Input as well as the Pass transistor Logic. In conclusion of Power dissipation and delay it analyzed that the performed data of adder of hybrid is varies in between the PTL and the GDI. On increasing the supply voltage of input, the characteristics of hybrid adder also changes. Due to the deficiency of voltage source (Vdc), the GDI and PTL do not produce the output of full swing. On increasing the supply voltage of input (Vp) extra voltages is required for the transmission from input to output through which the other transistors can easily executed.

4. Low Power Technique in Domino Logic Circuit Neha Vaish, Sampath Kumar V, 2018

In this paper, a new procedure is for diminishing the power absorption and developing the speed beyond reacting the noise margin is reviewed. In this paper, a technique of threshold voltage of the keeper transistor is diverse utilizing body bias generator circuit. In this paper, 3 different body bias generator circuits are implemented which are:- Dynamic Body Bias Generato

r• Capacitive Body Bias Generator

- Cross Couple Capacitive Body Bias Generator
- For carry look-ahead adder,

simulations are done on tanner EDA tool at 65nm as well as 180nm technology. The simulations output read presents that Capacitive Body Bias Generator (CBBG) and cross couple capacitive body bias generator (CCCBBG) decreased less power consumption and propagation delay as compared with another circuit architectures. In this paper, the dynamic body bias generator with double supply voltages develops the keeper transistor's threshold voltage by changing the substrate biasing of the keeper transistor. Dynamic body bias generator with triple supply voltage develops body bias voltage for the keeper transistor decreasing the power absorption beyond reacting noise margin. Capacitive body bias generator changing the voltage of capacitance C develops variable body bias voltage and it also develops a voltage which is two times more than the applied voltage.

5. Analysis of Full Adder using Adiabatic Charge Recovery Logic Amalin Marina, S Shunbaga Pradeepa T, Dr. A Rajeswari, 2017

This paper shows the correlative study of full adder utilizing various adiabatic logic architecture. Power analysis is executed at 45nm for various frequencies and output represents that at less frequencies Efficient Charge Recovery Logic (ECRL) absorbs 69% minimum power as compared it with the conventional CMOS logic design whereas at higher frequencies the power consumption of Secured-Quasi Adiabatic logic possess 71.8% lesser as compare it with the CMOS. SQAL is the advancement over ECRL. Analysis represents that the ECRL is capable at less frequencies as well as it represents minimum in power of 68% in comparison with CMOS whereas SQAL is more capable at maximum frequencies and it represents the decrease in power of 71%in comparison with conventional CMOS logic style. For architecture of full adder there are two relationship accesses which are: Static• Dynamic• A dynamic full adder is faster and more compact, consumes less silicon area, but it consumes more power and more sensitive to noise as compared to static full adder. That's why for designing a 1- bit full adder cell, we use domino logic style and after comparison with the static

logic which is depend on 28T full adder cell and 10T full adder cell and also correlated with the 27T domino full adder cell.

6. Modified Positive Feedback Adiabatic Logic for Ultra Low Power Adder Shiv Pratap Singh Kushawaha, Trailokya Nath Sasamal, 2019

This paper recommend Modified Positive Feedback Adiabatic Logic (MPFAL) which is utilize for ultra-low-power circuits. MPFAL is depend upon positive DC voltage ranging from 0.1V-0.3V. Half Adder and 1-bit full adder consolidate this technique used for the low power circuits. After compared between these two techniques, we concluded that the average power is minimized in case of Modified Positive Feedback Adder as compared to the Positive Feedback Adiabatic Logic All the simulations are executed in Cadence Virtuoso Tool utilizing UMC 180nm CMOS Technology. This technique can be utilized in ultra-low power digital circuits executed in maximum frequencies.

7. Energy Efficient Low Power High Speed Full Adder design Using Hybrid Logic M Nikhil Theja, Dr T Balakumaran

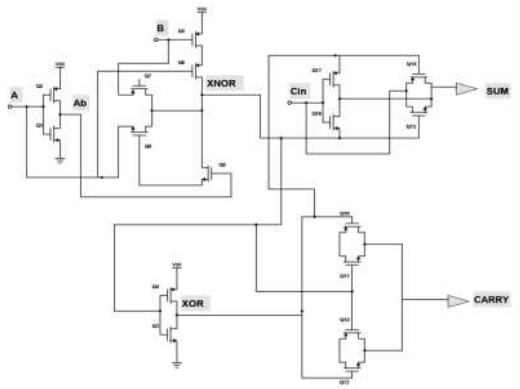
In this paper, hybrid logic architecture utilize to construct the full adder. The prime goal of this architecture is, complete maximum speed as well as minimum power. Hybrid logic style utilize the combination of C-CMOS logic (Complementary Metal Oxide Semiconductor) and Transmission Gate (TG) logic. The circuit was appliance using Micro-wind tool in 90nm as well as 180nm Technology. Average power absorption of the proposed architecture is organized to 1.114W at 90nm technology for 1.2V supply and 5.641W at 180nm for 1.8V supply. Delay in the signal propagation is calculated as 0.011ns and 0.087ns for 90nm and 180nm technology. Thus absorbing extremely low power and depend upon minimum time in comparison to the existing architecture for the double testing status. Power delay product (PDP) is measured as product of Power and Delay digits represent energy demand of the architecture. Proposed architecture needs 71% minimum energy in comparison to TFA and 81% minimum energy than TGA and 92% minimum energy in comparison to conventional CMOS-adder.

8. Adiabatic Logic: An Alternative approach to Low Power Application Circuits Preeti Bhati, Navaid Z. Rizvi, 2020

In this paper, there is a comparison between PFAL Logic and CMOS Logic is executed at various voltages and frequencies. PFAL is also known as Partial Energy Recovery Circuit because it possess a great robustness. It is also known as the dual-rail circuit. In this paper, 1-bit sum and carry adder are fabricated and simulated on CADENCE VIRTUOSO using 180nm Technology. The Adiabatic logic has become a solution of the question of power dissipation. The proposed technique represents the minimization of power dissipation in comparison with the conventional CMOS architecture style switching events. We concluded that the power dissipation in PFAL is less as compare with the conventional CMOS logic circuits. PFAL logic architecture shows the significant power minimization and gives the better performance results as compared with the conventional CMOS logic. Although PFAL go through the great switching period, therefore it is not suitable when the delay is critical.

OBSERVATION ON EXISTING FULL ADDERS

The first hybrid full adder is 17T FA. The 17T FA circuit consists of three stages and 17 transistors. On the first stage CMOS inverter is there that inverts the input A. The next stage uses low power XNOR circuit in which B input is applied. XOR is obtained by inverting XNOR in stage 2.Finally, at stage 3 GDI MUX produces output SUM while TG output produces COUT.



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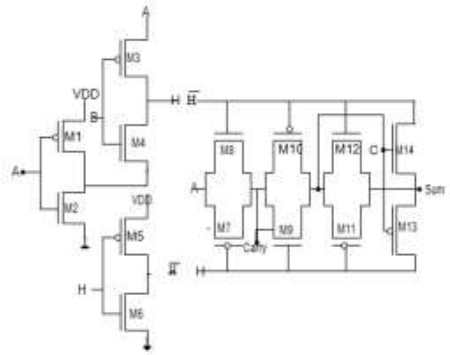
GDI MUX is connected with a TG for swing restoration. As we have studied GDI technique exhibit voltage drop, hence to restore it TG is attached at the output of GDI MUX.N17T FA circuit is shown in figure.

III. EXISTING RIPPLE CARRY ADDER

The N-bit two operand adder is known as ripple carry adder (RCA). These are referred as chain structure. In the regular design approach, which is nothing but the conventional approach, the carry ripples from first (LSB) 1-bit full adder to last one (MSB). Hence there is a large loading on LSB input so that there is an increase in delay and PDP results. The depicts a basic flow diagram of 4-bit RCA in regular approach. Here the red dotted line shows the worst propagation path which is the possible longest path over which the input C0 travels to provide sum and carry at the output stage that results in large loading on the carry. While the blue dotted line shows the intermediate propagation path. The worst propagation path starts from first adder cell till last which results in large loading on LSB input i.e. C0.

The second proposed full adder is N14T FA. In N14T FA circuit, fourteen transistors make a full adder in the form of cascaded output structure. The N14T FA is based on 4T-XOR function, CMOS inverter, TG and pass-transistor logic. In the N14T FA topology, XOR function is designed using four transistors as shown in fig. 1and subsequently, XNOR function can also be implemented using CMOS inverter. N14T FA circuit is shown in Fig. .

Two input 4T-XOR function H(A□B) is implemented with the four transistors (M1, M2, M3 and M4). Similarly, two input 4T-XNOR function is implemented by addition of CMOS inverter transistors (M5, M6) to the 4T XOR. The complementary outputs of the XOR and XNOR gates are used to control the transmission gate which together realizes a multiplexer circuit producing the Carry function. Aspect ratio of the inverter circuit must be high for high driving capabilities. The output logic of four transistor based XOR function followed by TG & PT based multiplexers are used to design Sum and Carry functions in the proposed full adder topology.



N14T FA circuit

IV. PRPOSED METHOD

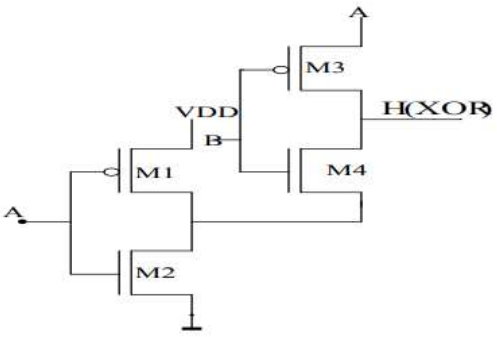
HYBRID FULL ADDER CIRCUITS TOPOLOGIES

In this hybrid full adder architecture N17T and N14T are proposed. 4T XOR logic function is designed using four transistors as shown in Figure and subsequently, XNOR function can also be implemented using CMOS inverter. Following Boolean equations are employed to generate XOR and XNOR signals are:

$$A\bar{B}+\bar{A}B=XOR$$

$$\overline{XNOR}=XOR$$

XOR and MUX logic circuits implemented have shown correct logic at all input logic conditions and schematic diagram as shown in Figures respectively.

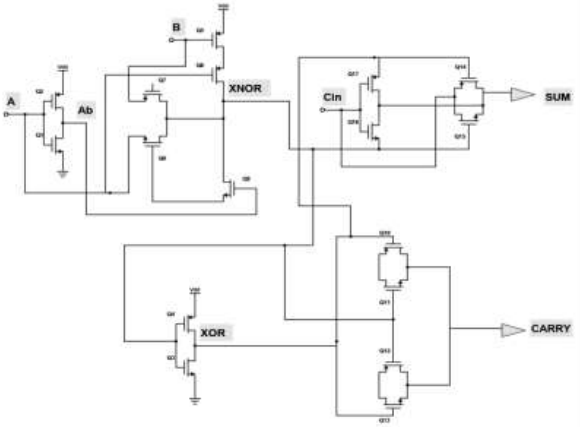


14T XOR logic circuit

The functionality of the full adder topology is based on the following Boolean equation:

$$Sum = Cin(A \oplus B) + Cin(A \odot B)$$

$$Carry = (A \odot B)Cin + (A \odot B)B$$



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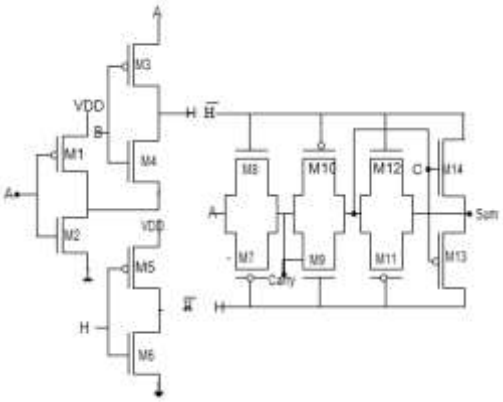
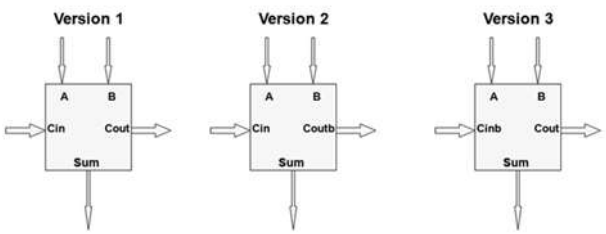


N14T FA circuit

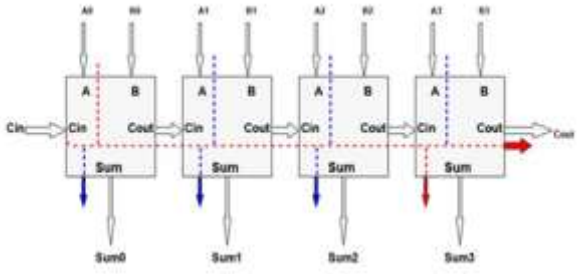
REGULAR AND Modified TRIPLET LOGIC DESIGNAPPROACH

The triplet design approach aims to improve the drive strength of adder by breaking the propagation path of input Cinthereby reducing loading problem. In this approach, we use the three different versions of the 1-bit full adder cell as presented in Figure.

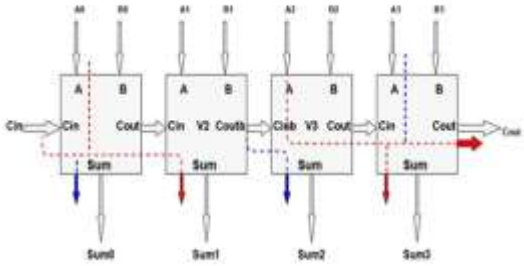
- **Version 1**: It is basic adder where A, B and Cin act as input and Sum and Cout act as output.
- **Version 2**: It is an adder where A, B and Cin act as input and Sum and inverted Cout (Coutb) act as output.
- **Version 3**: It is an adder where A, B and inverted Cin (Cinb) act as input and Sum and Cout act as output.



Triplets FA design approaches



4-bit RCA regular design



4-bit RCA triplet design

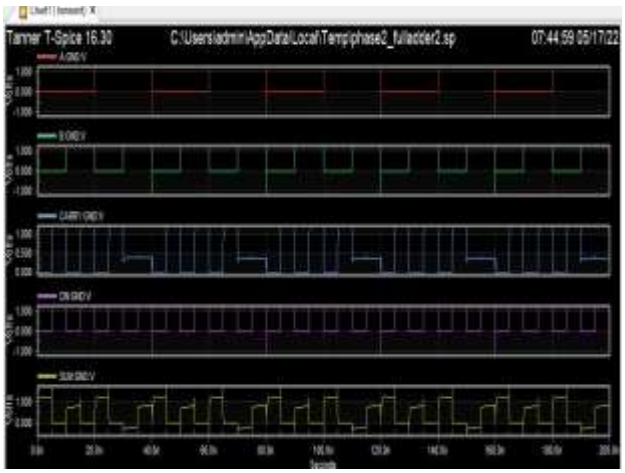
Proposed or modified Triplet design of Ripple Carry Adder

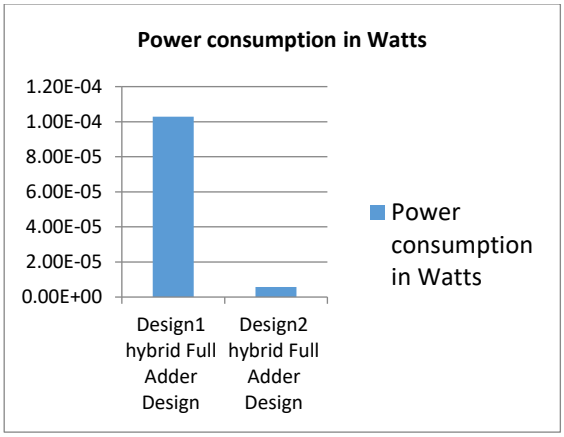
Triplet logic design approach based 4-bit RCA drawn shown in Figure. Here, the first and fourth block of the adder are basic adders as discussed in Version1, whereas second and third block are Version 2 and Version 3 respectively. From figure, we notice that the longest critical path that is the red dotted line is reduced to only two stages unlike the regular where the critical path goes through all stages. The propagation path is cut because of the inverted carry output of version 2 adder at the second stage that results in independency of carry output of second stage on C0 and hence critical path reduces to only two stages. This reduces the loading problem and improves the driving strength of the adder without any additional buffer requirement.

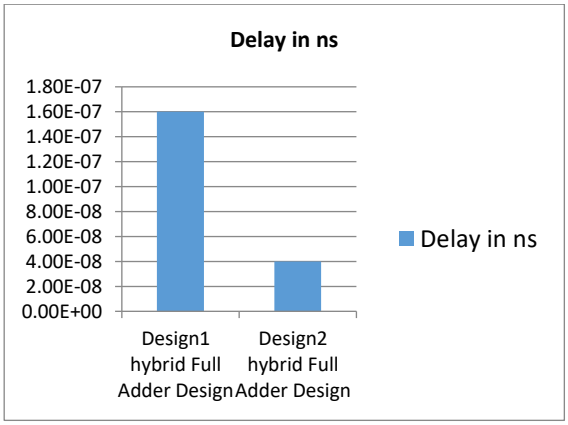
V. Output Results

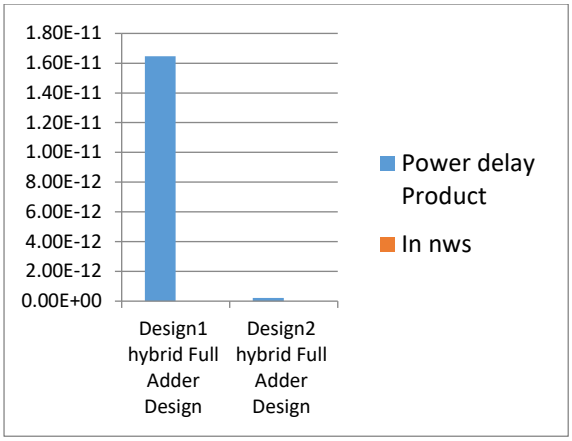
Comparsion results for PHASE2 design

S.No	Parameters	Design1 hybrid Full Adder Design	Design2 hybrid Full Adder Design
1	Power consumption in Watts	1.02933 4e-004	5.64818 6e-006
2	Delay in ns	1.60002 e-007	4.0002e -008
3.	Transistor Count	17	14









VI. CONCLUSION

In this hybrid full adders topologies has been proposed for high speed and low power VLSI application. The proposed N14T adder has shown the best performance in terms of lowest PDP compared to its counterparts. There is a significant power reduction in the proposed adder circuits without affecting the other parameters. This is the plus point of using the hybrid design style technique, which reduces the power dissipation to great extent thereby improving the PDP. Thus, a pathway is created to use the hybrid low power techniques in other computational devices where power reduction is main requirement in nanotechnology application. 4-bit RCA hybrid full adders has been designed by regular design and triplet design approach using all five adders topologies and have been analyzed at from supply voltage V_{DD} 0.6 to 1.2V. From the simulation results analysis of 4-bit RCA, we see that N17T and N14T adder has shown least power and PDP from the other implemented reference circuits. The simulation results reveal that the Triplet logic approach design topology has topology has successfully improved the performance of RCA by breaking the propagation path in the chain structures. This design approach improves the drive strength of full adder and hence eliminates the requirement of buffers. This design achieves low PDP in all the cases compared to regular design making it very suitable to utilize it in battery operated devices.

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