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FPGA Realization of 2D Convolution for High Speed Image Processing Applications

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Abstract

Extracting the information from the image with high throughput rate plays a vital role in present scenario. In spatial domain analysis the design of mask/filter has a prominent role in the processing of images. The two dimensional convolution has different applications in digital image processing. The 2 Dimensional Convolution filtering is a technique which can be used for a large group or many of image processing techniques that can includes sharpening of an image, image smoothing, edge detection and analysis of texture. The main intention of this work is to develop an efficient architecture for the 2 dimensional convolution by using the control blocks. Hardware implementation can be realized such that there is reduction in number of multipliers, shift registers, control blocks and adders of this 2 dimensional algorithm. It leads to architecture with fewer number LUTs and hardware is also becomes less. In generally the computational complexity increases if the size of the mask is increases due to this the architecture for the model also vary. The proposed work aims at performing the image denoising or edge detection from the input images based on the user requirement. The proposed 2 dimensional convolution architecture approach is faster compared to the existing 2D convolution implementation and maximum time required after clock time is less when compared to the existing 2D convolution.

Keywords : 2D convolution , Image processing , Denoising

1 Introduction

An image can be figured as a two dimensional function which is given by f(x, y). In the image function f(x, y), x and y are termed as spatial coordinates or plane coordinates. If the image is with a finite number and discrete coordinates along with

the discrete grey level values then the image is termed as the digital image. For a given function f (x, y) the amplitude of it at particular coordinates is termed as its intensity at that particular point. Thus the digital images are treated as combination of finite elements and these are given as pixel values.

These finite elements have particular locations and values. Thus the digital image processing is termed as processing of digital images by digital computer. These images plays as major aspects in human day to day life applications given as agriculture, industry, satellite television and medical field. In research and technology fields such as geographical information areas and astronomy also used [2].

When the digital image processing techniques are taken into considerations while dealing with several techniques, the filtering operation is commonly and popularly used technique in many fields for the purpose of enhancing of an image. The filtering operation a technique that can be used to perform denoising from images or remove the noise from images and to obtain necessary features in image. Generally, filtering is carried out with help of a filter mask and this mask is convoluted with image. Thus filtering technique can be achieved through convolution operation.

When filtering operation is considered the low pass filters are mainly considered to eliminates high frequency components and retains or acquire low frequency components. And these filters also used to get smoothed version of the image i.e. image smoothening. These filters can enhance the edges and the constant background information can be suppressed. The high pass filters are used to retains high frequency components and remove low frequency components. A high-pass filter widely used to convert the image as sharper i.e. image sharpening. These filters find the fine details of the image which is exactly the opposite compared with low pass filter [15].

2 2D Convolution

The two dimensional convolution filtering is a operation which can be used in most commonly used image processing techniques which can includes sharpening of an image, image smoothing and edge detection [4] [8]. So that the two dimensional

convolution algorithm high degree of significance in techniques of image processing. To perform the filtering sub array of matrix is used which is given as kernel and is also called as mask. In generally kernel nothing but small array which is convolute by each and every pixel along its neighboring within the image. The image is convoluted with kernel to obtain [5].

The mathematical equation for convolution operation can be defined as mentioned, it can be defined as the mask is convolved with an image.

$$F(x,y) = h(x,y) * f(x,y) \quad (1)$$

The mathematical equation of convolution filtering is given as below,

$$F(x,y) = \frac{\sum_{x=1}^{3}\sum_{y=1}^{3} f(x,y).h(x,y)}{\sum_{x=1}^{3}\sum_{y=1}^{3} h(x,y)}$$

In the above expression the image pixel values represented by the f(x, y), kernel convolution matrix represented by the h(x, y) and resultant of the convolution is represented by the image matrix F(x, y). The each value of the mask is multiplied with the corresponding pixel. Then multiplied values are added and write the resulting value in the center pixel as a the new value. And this process is continued across the total image until total pixel values are taken. The convolution of the pixel value is zero when pixel value of the kernel is outside of the matrices.

P1	P2	P3	P4
P5	**P6**	P7	P8
P9	P10	P11	P12

P13	P14	P15	P16

Fig. 1. Image resolution matrix

K1	K2	K3
K4	K5	K6
K7	K8	K9

Fig. 2. Kernel matrix

R1	R2	R3	R4
R5	**R6**	R7	R8
R9	R10	R11	R12
R13	R14	R15	R16

Fig. 3. Convolution result matrix

Let consider the 3x3 image kernel or mask matrix and a image whose size is 4x4. With the help of above matrices the convolution is performed for those matrices then size of resultant matrix is given by 4x4. In case of given input image for convolution operation the pixel value P6 (bolded) is considered and the kernel values are placed on the image and it is multiplied with center pixel and corresponding neighbor pixels. All the values are added and resulting array has same elements size as the mask and are averaged.

The following equation is shows how convolution is performed,

$$R6 = (P1\times k1) + (P2 \times k2) + (P3 \times k3) + (P5 \times k4) + (P6 \times k5) + (P7 \times k6) + (P9 \times k7) + (P10 \times k8) + (P11 \times k9) \quad (2)$$

As per the above equation mentioned the R6 value is calculated in convolution. The same procedure follows to calculate the values of R1, R2, R3, R4, R5, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16. As the image resolution is more and more, then in convolution operation the mean multiplication and additions also increases due to this propagation delay also increases. If size of the kernel going to be high then number of additions and multiplications are increases due to this computational complexity also increases. Because of this when compared to 5x5 kernels 3x3 kernel is widely used. But if the image is highly effected by the noise then 3x3 kernel is not suitable to remove the noise then kernels with high orders are used.

Let consider a Gaussian filter 7x7 which is very useful to suppress more noise when compared with the 3x3 Gaussian kernel. In accordingly when compared with 3x3 the 7x7 Gaussian filter can blur out the edges more.

3 Proposed Method

In this section the proposed architecture is discussed. It is used to perform the convolution operation and the architecture of proposed design is as shown in below fig. The write control block and read control block are the two major blocks in this architecture. The proposed architecture also contain the ALU block and pipelining shift registers [3]. In this architecture the size of the pipelined shift register 1 and the pipelined shift register 2 dependent on the image resolution. Each shift register consists of eight bits depending upon the operation these registers pixel values are moved one by one. Let consider an example, the image resolution is given by 4x4 then six registers are allotted to pipelined shift register and six registers are allotted to the pipelined shift register 2 .The both registers are with eight bits each [1].

The pipelined shift register 3 contain only three registers. The allocation of the registers is independent of the image resolution in the pipelined shift register 3

because the size of the kernel matrix is 3×3. The pipelined shift register 3 has nine registers for the kernel matrix whose size is 9×9 with each register has the eight bits. The assumption gives the clarification that the kernel size be decides the pipelined shift register 3 register allocations than the image resolution [1].

The read control block consists multiplexers, ROM memory along with counter. The write control block also contain the multiplexer, register and AND gate. To perform the convolution operation the kernel is shift over the entire image. The input to architecture are several pixel values and output is calculated for those inputs respectively. The input to the shift registers are image pixel values and shift registers in pipelining structure are used for the purpose of moving pixel values sequentially.

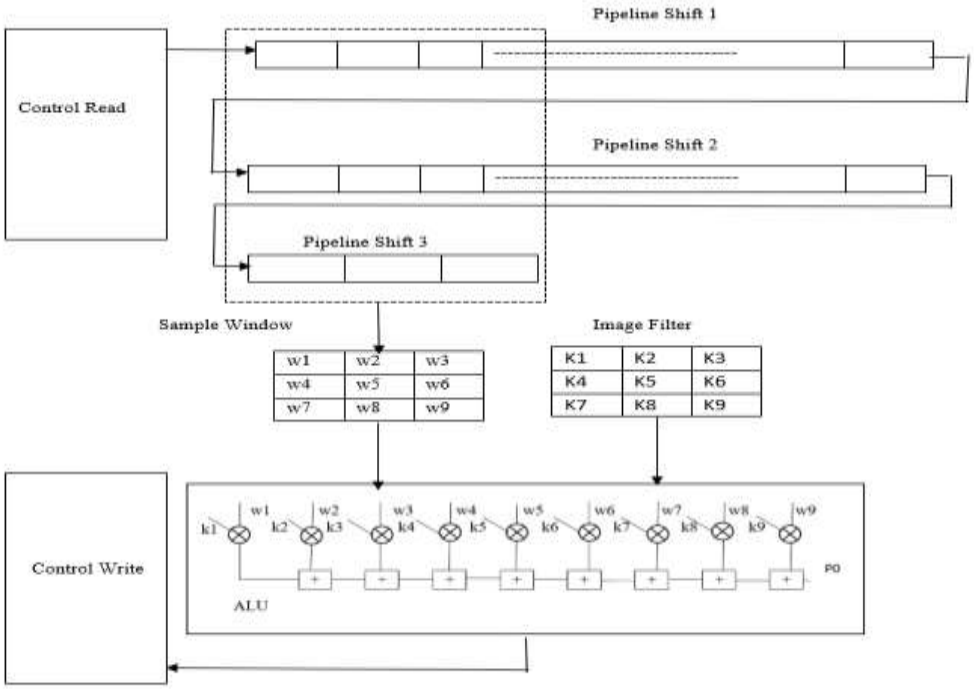

Fig. 4. The proposed architecture

` In to the shift registers after the completion of every line the two zeros are added. A multiplexer is helps to addition of zeros as shown in below fig. Here, zero padding on the entire image is used to enable the spatial filtering [6].

In this work the low pass filter and high pass filters are designed to perform image smoothing and image sharpening respectively. In image smoothing noise is reduced and suppressed. In image sharpening fine details are highlighted in the image and used to enhance the high-frequency components.

The following fig shows the low pass filter kernel , which is 3x3 kernel matrix and it has all the values as equal and positive pixel values,

$$1/9 \times \begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix}$$

Fig. 5. Low pass filter kernel

The following figure shows the example for the high pass filter kernel, which is 3x3 kernel matrix. In this matrix sum of the all kernel values are equal to zero. In this matrix all the values are negative and center pixel value is positive pixel value.

-1	-1	-1
-1	8	-1
-1	-1	-1

Fig. 6. High pass filter kernel

The above mentioned mask is used to perform the denoising of image and also to perform the edge detection of an image.

4 RESULTS AND DISCUSSION

In this work the image filtering operation that can be implemented by using the kernel matrices of convolution is low pass filtering operation ,

1/9	1/9	1/9
1/9	1/9	1/9
1/9	1/9	1/9

Fig. 7. Low filter for image kernel

The representation of low pass filter kernel is given in above figure and it is also called as the smoothing filter. This filter is performs the reduction of high frequency information while retaining the low frequency information within the

image. This low pass filter also used to performing the image denoising from input images or reduce the noise content from image which is depending upon requirement of user. In generally the disparity between pixel values of an image is decreased which leads to smoothing operation.

This low pass filter is also known as blurring filter which replaces the original pixel value by average values of the pixel. The order of designed low pass filter kernel/mask filter be 3x3. The following figure shows the input test image of size 128x128 which is applied to low pass filter ,

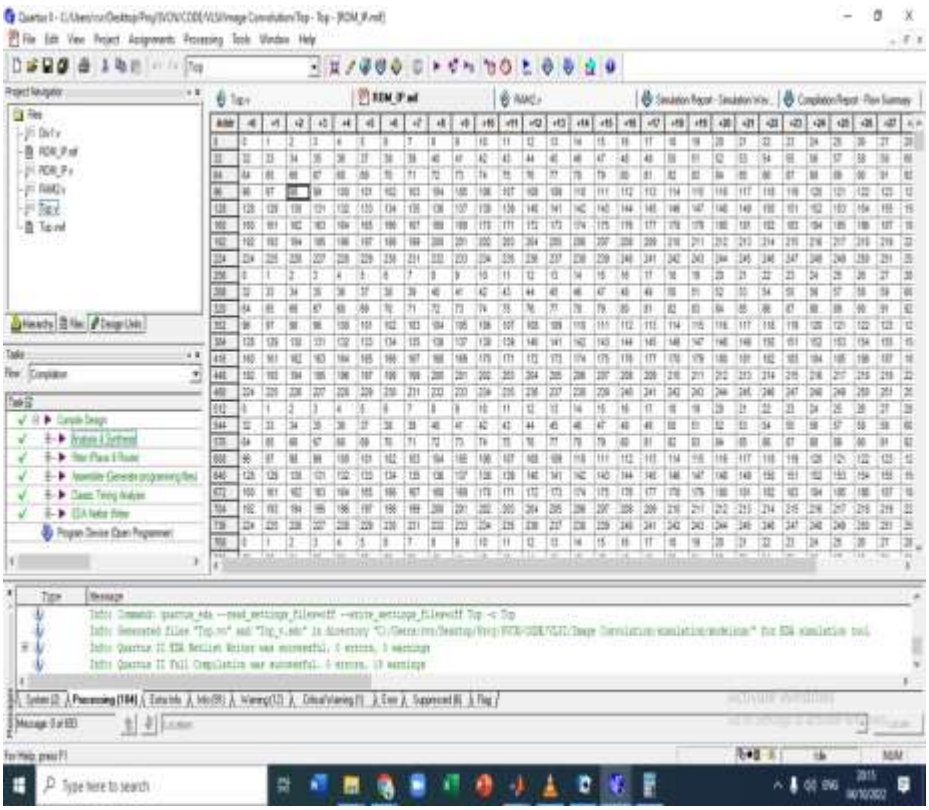

Fig. 8. Input image pixel values

After giving the input image pixel values to filter the output image pixel values which are obtained are as shown in below fig,

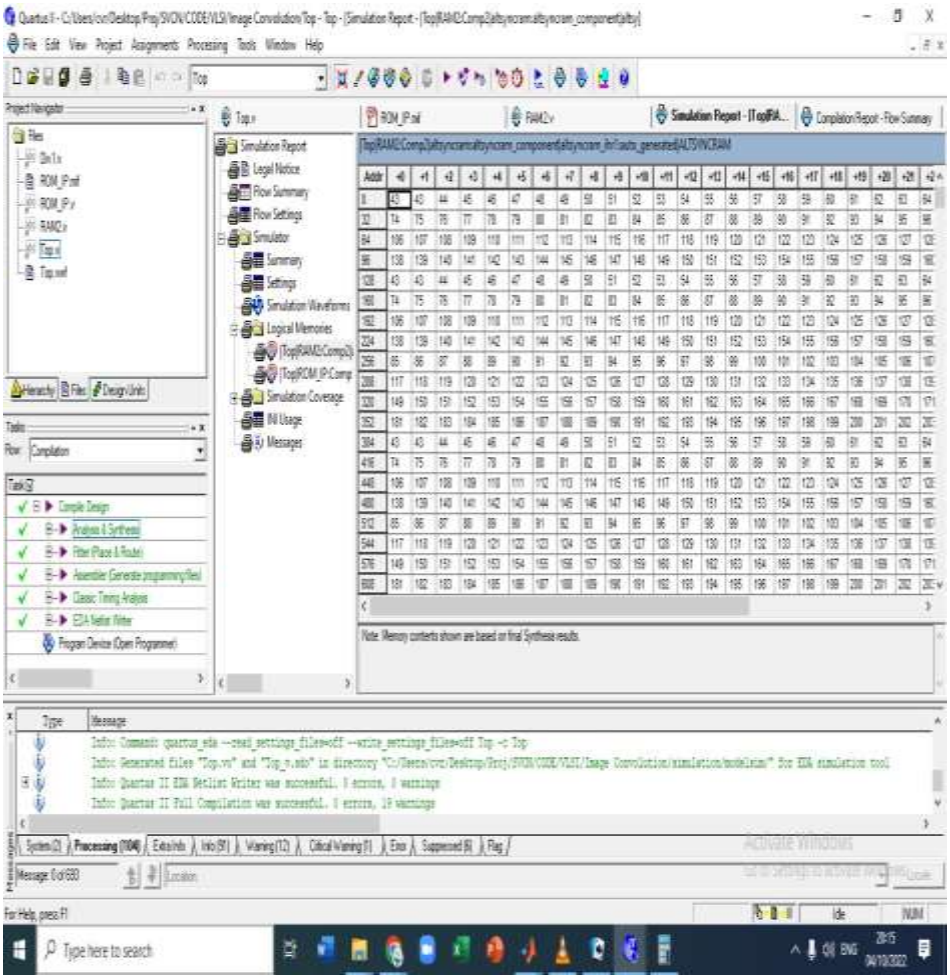

Fig. 9. Output of convolution store in memory

4.1 SIMULATION RESULTS

In this section the convolution operation simulation results and its output is showed in below fig's. And also the compilation report of flow summary simulation waveforms are showed in below figures,

The simulation waveforms for the convolution operation are showed in following figures in terms of nano and micro seconds respectively,

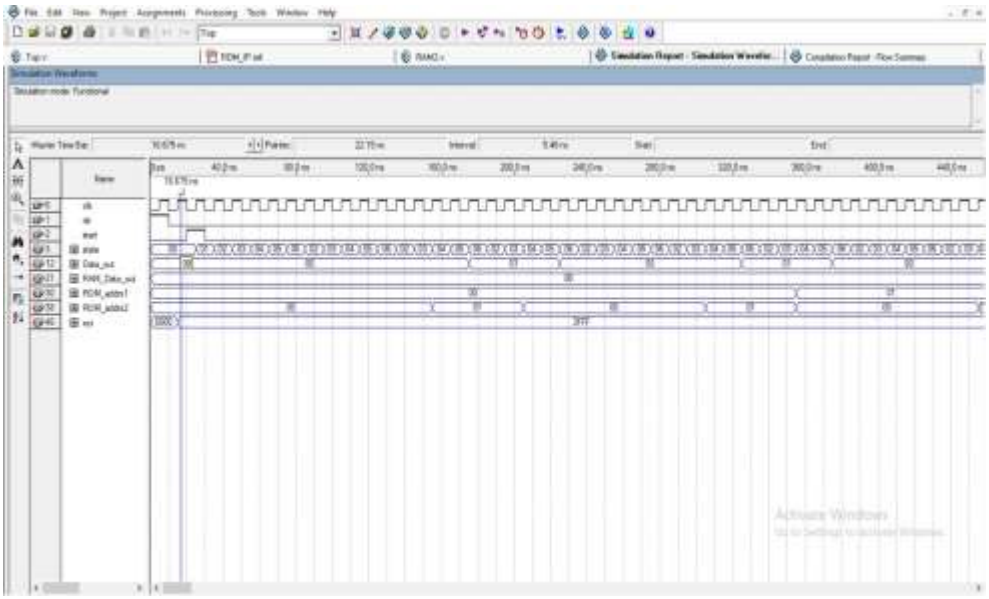

Fig. 10. Simulation wave form(ns)

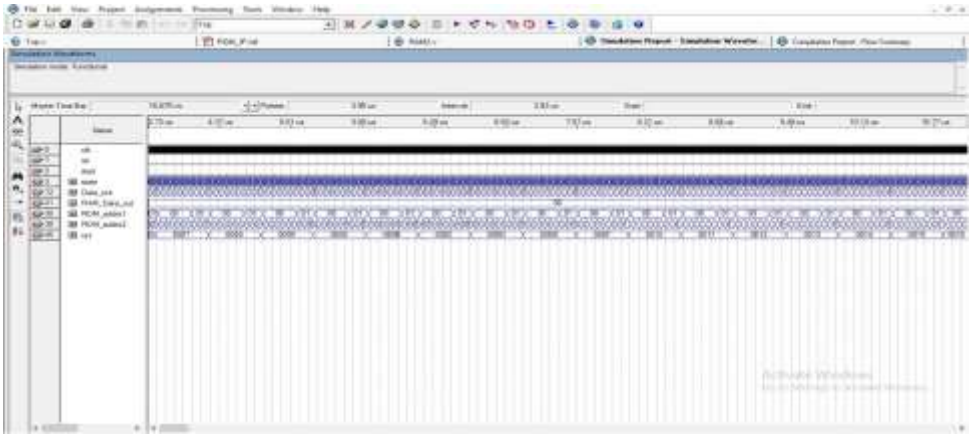

Fig. 11. Simulation wave form(us)

The comparison table for the design with DIV operation and without DIV operation is as shown in below table ,

	No. of LUT tables	**Operating frequency (MHZ)**
With DIV operation	457	44
Without DIV operation	600	122

Table. 1. The comparison table

From above table the no. of LUT's required for design with DIV operation be 457 whether for design without DIV operation be 600. And the operating frequency for design with DIV operation be 44 MHz whether for design without DIV operation be 122 MHz's.

5 CONCLUSION

In this work the FPGA realization of 2D convolution for high throughput image processing application has been implemented. It is an simple and efficient hardware

implementation which consisting of very less number of LUT's due to this the area of design is reduced. The implementation of this architecture gives the high area reduction when compared to previous design .Because of this high amount of hardware saving in designing of this block. And the low pass filter was used to smoothen the image information and this is also help to reduce noise content in image. Thus multiple units of pipelined architecture can be implemented for making it possible for processing images in real time life.

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